REMARKS

The Examiner is thanked for the thorough examination of this application, and the removal of the previous rejections. The Office Action, however, continued to reject all claims 1-15.

Rejection under 35 U.S.C 102(b)

Claims 1-4, 6, 8, 10 and 12-15 stand rejected under 35 U.S.C 102(b) as allegedly anticipated by Tseng et al. (US 6,528,402). With regard to the 35 USC 102(b) rejections, it is respectfully Applicant first refers to independent claim 1, which recites:

> 1. A method of forming an integrated circuit transistor, comprising:
> providing a semiconductor substrate with a gate structure formed thereon;
> forming at least one dielectric layer overlying the semiconductor substrate, ***wherein the at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure, and at least one second portion outside the gate structure along the surface of the semiconductor substrate***;
> forming at least one first doped region in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one dielectric layer, wherein the at least one second portion of the at least one dielectric layer remains overlying the at least one first doped region;
> forming a sidewall spacer overlying the at least one dielectric layer along the at least one sidewall of the gate structure; and
> forming at least one second doped region in the semiconductor substrate laterally adjacent to the sidewall spacer.

Similarly, independent claim 10 recites:

> 10. A method of forming a semiconductor device, comprising:
> providing a semiconductor substrate with a gate structure formed thereon;
> blanket depositing at least one first dielectric layer overlying the semiconductor substrate without performing an etch process on the at least one first dielectric layer;
> wherein, the at least one first dielectric layer comprises at least one first portion along at least one sidewall of the gate structure;
> ***wherein, the at least one first dielectric layer comprises at least one second portion outside the gate structure along the surface of the semiconductor substrate;*** and
> performing a first ion implantation process to form at least one first doped region in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one first dielectric layer, wherein the at least one second

portion of the at least one first dielectric layer remains overlying the at least one first doped region.

(*Emphasis added.*) Independent claims 1 and 10 patently define over the Tseng reference for at least the reasons that Tseng fails to disclose the features emphasized above.

In contrast, Tseng discloses a dual salicidation process. The dual salicidation process includes a semiconductor substrates 40, a gate dielectric 42 formed on the substrate 40, a polysilicon gate conductor 44 patterned on the polysilicon gate conductor 44. And a poly-gate spacer 50 is only formed laterally adjacent the sidewall of the gate conductor 44. However, **the gate dielectric 42 doesn't have a portion along at least one sidewall of the gate structure 44.** Although the poly-gate spacer 50 is formed laterally adjacent the sidewall of the gate conductor 44, **the poly-gate spacer 50 is not the portion of the gate dielectric 42**.

Accordingly, Tseng et al. does not teach that the **at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure, and at least one second portion outside the gate structure along the surface of the semiconductor substrate**. Since Tseng fails to teach the claimed features above of the claims 1 and 10, claims 1 and 10 are allowable. Insofar as claims 2-9 depend from claim 1, claims 12-15 depend from claim 10, these claims are also allowable.

Rejection under 35 U.S.C 103(a)

Claim 5 stands rejected under 35 U.S.C 103(a) as allegedly unpatentable over Tseng et al. (US 6,528,402) in view of Samavedam et al. (6423632). Claim 7 stands rejected under 35 U.S.C 103(a) as allegedly unpatentable over Tseng et al. (US 6,528,402) in view of Perng et al. (US 6,498,067). Claims 9 and 11 stand rejected under 35 U.S.C 103(a) as allegedly unpatentable over Tseng et al. (US 6,528,402) in view of Schuegraf et al. (6,140,203).

With regard to the 35 USC 103 rejection, it is noted that Samavedam discloses a semiconductor device and a process for forming the same. At least one dielectric layer 52 is a blanket deposition by a chemical vapor deposition (CVD) process using tetraethylorthosilicate (TEOS). Perng discloses an anisotropic RIE procedure for the second insulator layer 6a etching. Schuegraf discloses a layer 48 is characterized by a wet etch rate of about 75 Angstroms/minute in a 100:1 by volume H_2O: HF solution.

In particular, Applicant respectfully asserts that the cited references, either individually or in combination, are legally deficient for the purpose of rendering obvious the **at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure, and at least one second portion outside the gate structure along the surface of the semiconductor substrate** recited in independent claims 1 and 10. Specifically, Applicant respectfully asserts that *Tseng, Samavedam, Perng* and/or *Schuegraf* do not teach or reasonably suggest at least the **at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure, and at least one second portion outside the gate structure along the surface of the semiconductor substrate** emphasized above in claims 1 and 10. Additionally, the offset spacer is formed by a blanket deposition of the first dielectric layer without extra photolithography and dry etch processes prior to an LDD ion implantation process. And the second portion of the first dielectric layer remains on the LDD region during the ion implantation process to prevent silicon loss and dosage contamination.

Therefore, claims 1 and 10 are allowable. Insofar as claims 5, 7, 9 depend from claim 1, and claim 11 depends from claim 10, these claims are also allowable.

As a separate and independent basis for the patentability of claims 5, 7, 9, and 11, Applicant respectfully traverses the rejections as failing to identify a proper basis for combining the cited references. In combining the references Tseng and Samavedam references, the Office Action stated only that the combination would have been obvious "because TEOS can be use to isolation of gate in the semiconductor transistors (*sic*)." (Office Action, page 4). In combining the references Tseng and Perng references, the Office Action stated only that the combination would have been obvious "because dry etch is used for an isotropic etch for sidewall." (Office Action, page 5). In combining the references Tseng and Schuegraf references, the Office Action stated only that the combination would have been obvious "because TEOS density can also be characterized relative to an etch rate of about 175 Angstroms/minute." (Office Action, page 5). These alleged motivations are clearly improper in view of well-established Federal Circuit precedent.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicant notes that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a sidewall spacer, as claimed by the Applicant.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000). The rationales relied on by the Office Action in the present application are merely generic statements, that have nothing to do specifically with the structures disclosed in the other references. As such, these rationales cannot be properly viewed as proper motivations for combining the specific teachings of the individual references. Indeed, the generic motivations advanced by the present Office Action could be used to support a combination of ANY references, which is clearly contra to the cited Federal Circuit precedent and the clear intent of 35 U.S.C. § 103.

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejections under 35 U.S.C. § 103, those rejections should be withdrawn.

For at least the foregoing reasons, all claims 1-15 are believed to be in condition for allowance, and the Examiner is respectfully requested to pass those claims to issuance. If the Examiner believes a teleconference will expedite the examination of this application, the Examiner is invited to contact the undersigned attorney at 770-933-9500.

No fee is believed to be due in connection with this Response to Office Action. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to deposit account 20-0778.

Respectfully submitted ,

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